

We claim:

1. A computer storage medium comprising a stored VLIW instruction, which instruction comprises a plurality of operations for commencing execution in a same machine cycle on distinct functional units of a VLIW processor, each non-null operation being compressed according to a compression scheme which assigns a compressed operation length to that operation, the compressed operation length being chosen from a plurality of finite lengths, which finite lengths include at least two non-zero lengths, which of the finite lengths is chosen being dependent upon at least one feature of the operation.

2. The medium of claim 1 wherein the set of operation lengths is {0, 26, 34, 42}.

3. The medium of claim 1 wherein the at least one feature is at least one of the following:

- abbreviated op code;
- guarded or unguarded;
- resultless;
- immediate parameter with fixed number of bits; and
- zeroary, unary, or binary.

4. The medium of claim 3 wherein combined operation types are aliased according to the following table

FORMAT	ALIASED TO

zeroary	unary
unary_resultless	unary
binary_resultless_short	binary_resultless
zeroary_param32_short	zeroary_param32
zeroary_param32_resultless_short	zeroary_param32_resultless
zeroary_short	unary
unary_resultless_short	unary
binary_resultless_unguarded	binary_resultless
unary_unguarded	unary
binary_param7_resultless_unguarded	binary_param7_resultless
unary_unguarded	unary
binary_param7_resultless_unguarded	binary_param7_resultless
zeroary_unguarded	unary
unary_resultless_unguarded_short	binary_unguarded_short
unary_unguarded_short	unary_short
zeroary_param32_unguarded_short	zeroary_param32
zeroary_param32_resultless_unguarded_short	zeroary_param32_resultless

zeroary_unguarded_short	unary
unary_resultless_unguarded_short	unary
unary_long	binary
binary_long	binary
binary_resultless_long	binary
unary_param7_long	unary_param7
binary_param7_resultless_long	binary_param7_resultless
zeroary_param32_long	zeroary_param32
zeroary_param32_resultless_long	zeroary_param32_resultless
zeroary_long	binary
unary_resultless_long	binary

5. The medium of claim 3, wherein the fixed number is one of 7 and 32.

6. The medium of claim 1 comprising a plurality of such instructions, of which one instruction is a branch target, which one instruction is not compressed.

7. The medium of claim 1 wherein each operation field within each instruction includes a sub-field specifying at least one of the following: a register file address of a first operand; a register

file address of a second operand; a register file address of guard information; a register file address of a result; an immediate parameter; and an op code.

8. The medium of claim 1 comprising a plurality of such instructions, each instruction comprising a format field for specifying a plurality of respective formats, one respective format for each operation of a succeeding instruction.

9. The medium of claim 8, wherein the compressed format comprises a format field specifying issue slots of the VLIW processor to be used by some instruction.

10. The medium of claim 9 comprising at least one field specifying the operation.

11. The medium of 9 wherein the format field has $2*N$ bits, where N is the number of issue slots.

12. The medium of 10 wherein the at least one field specifying the operation comprises at least one byte aligned sub-field.

13. The medium of claim 10 further comprising at least one operation part sub-field located in a same byte with the format field.

14. The medium of claim 9 wherein the instruction takes up no more than 32 bytes.

15. The medium of claim 1 comprising a plurality of such instructions, wherein at least two of the instructions have different lengths.

16. The medium of claim 1 wherein the instruction is aligned with a byte boundary, but not a word boundary.

17. The medium of claim 13 wherein the format field specifies that more than a threshold quantity of issue slots are to be used and further comprising at least one first operation part sub-field located in a same byte with the format field, a plurality of sub-fields specifying operations, and at least one second operation part sub-field located in a byte separate from the other sub-fields.

18. The medium of claim 9 formatted as follows

<instruction> ::=

<instruction start>

<instruction middle>

<instruction end>

<instruction extension>

<instruction start> ::=

<Format:2*N>{<padding:1>}V2{<2-bit operation part:2>}V1{<24-bit operation part :24>}V1

<instruction middle> ::= {{<2-bit operation part:2>}4 {24-bit operation part:24>}4}V3

<instruction end> ::= {<padding:1>}V5{<2-bit operation part:2>}V4 {24-bit operation part:24>}V4

`<instruction extension>::={<operationextension:0/8/16>}S`
`<padding>::= "0"`

Wherein the variables used above are defined as follows:

N = the number of issue slots of the machine, $N > 0$

S = the number of issue slots used in this instruction

$(0 \leq S \leq N)$

$C1 = 4 - (N \bmod 4)$

If $(S \leq C1)$ then $V1=S$ and $V2 = 2*(C1-V1)$

If $(S > C1)$ then $V1=C1$ and $V2 = 0$

$V3 = (S-V1) \text{ div } 4$

$V4 = (S-V1) \bmod 4$

If $(V4 > 0)$ then $V5 = 2*(4-V4)$ else $V5=0$

Explanation of notation

`::=` means "is defined as"

`<field name:number>`

means the field indicated before the colon has the
number of bits indicated after the colon.

`{<field name>}number`

means the field indicated in the angle brackets and
braces is repeated the number of times
indicated after the braces

`"0"` means the character "0"

`"div"` means integer divide

`"mod"` means modulo

`:0/8/16` means that the field is 0, 8, or 16 bits long.

19. The medium of claim 9 containing an operation which is encoded in 26, 34 or 42 bits, wherein

- if the operation is 26 bits, it is one of
 - binary unguarded short;
 - unary immediate 7-bit parameter unguarded operation;
 - binary unguarded immediate 7-bit operand resultless short; and
 - unary short;
- if the operation is 34 bits, it is one of
 - binary short;
 - unary immediate 7-bit parameter resultless short;
 - binary unguarded;
 - unary immediate 7-bit parameter unguarded; and
 - unary; and
- if the operation is encoded in 42 bits, it is one of
 - binary immediate 7-bit parameter resultless;
 - binary;
 - unary immediate 7-bit parameter;
 - zeroary immediate 32-bit parameter; and
 - zeroary, immediate 32-bit parameter resultless.

20. The medium of claim 9 wherein the operations are encoded according to the following table:

	24-bit operation part				2-bit part	Extension	Size
	bit position						
name	0-6	7-13	14-20	21-23	24-25	26-34-41	

26-format:							
< binary- unguarded- short >	src1[0:6]	src2[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]		26
< unary- param7- unguarded- short >	src1[0:6]	param[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]		26
< binary- unguarded- param7- resultless- short >	src1[0:6]	src2[0:6]	param[0:6]	opcode[0:2]	opcode[3:4]		26
< unary- short >	src1[0:6]	dst[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]		26
34-format:							
< binary- short >	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	dst[0:6] 0	34
< unary- param-7- short >	src1[0:6]	param[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	dst[0:6] 0	34
< binary- param7- resultless- short >	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	param [0:6] 0	34
< binary-un guarded >	src1[0:6]	src2[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] XL011	34

< binary- resultless >	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] X1001	34
< unary- param7-un- guarded >	src1[0:6]	param[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] SL111	34
< unary >	src1[0:6]	dst[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] XL101	34
42-format							
< binary- param7- resultless >	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] SXX100 param[0:6]	42
< binary >	src1[0:6]	src2[0:6]	guard{[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] XL0101 dst[0:6]	42
< unary- param7 >	src1[0:6]	param[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7] SL1101 dst[0:6]	42
< zeroary- param32 >	param [7:13]	param[0:6]	dst[0:6]	param [14:16]	param [17:18]	param [19:23] XX1 param [24:31]	42
< zeroary- param32- resultless >	param [7:13]	param[0:6]	guard[0:6]	param [14:16]	param [17:18]	param [19:23] 000 param [24:31]	42

< zeroary- param32- resultless >	param [7:13]	param[0:6]	guard[0:6]	param [14:16]	param [17:18]	param [19:23] 100 param [24:31]	42
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wherein:

S: signed/unsigned format bit for parametric operations; S=1 if signed, S=0 if unsigned

L: latency format bit; L=0 if (latency=1 and this is not a resultless operation) else L=1

X: undefined value

21. A computer storage medium comprising a stream of stored instructions for execution on a VLIW processor, the stream of instructions comprising:

- at least one first instruction which is a branch target and which is uncompressed; and
- at least one second instruction following the branch target which is compressed according to a scheme where formats are assigned to instructions according to features of the instructions.

22. The medium of claim 21 wherein the at least one first instruction is stored aligned with a word boundary.

23. The medium of claim 21 wherein the at least one second instruction is stored unaligned with a word boundary.

24. The medium of claim 22 wherein at least one of the at least one first instruction or the at least one second instruction specifies a plurality of operations for beginning in a same machine cycle.

25. A computer storage medium comprising a stream of stored instructions, the stream of stored instructions including

- a first instruction including a format field which specifies an instruction compression format; and
- a second instruction, following the first instruction, that is compressed according to the format field in the first instruction.